

WHAT IS CLAIMED IS:

1. A method of signal processing, said method comprising:
 - 2 receiving a composite signal having a first component and a
 - second component, the first component including a value during each of a
 - 4 series of time periods, and the second component including a value having a
 - first time relation to a corresponding value of the first component during each
 - 6 of the series of time periods;
 - producing a delayed second component including a value
 - 8 having a second time relation to a corresponding value of the first component
 - during each of the series of time periods; and
 - 10 multiplexing the values of the delayed second component and
 - the values of a component based on the first component onto a common signal
 - 12 path.
2. The method of signal processing according to claim 1, wherein
 - 2 the value of the delayed second component during each of the series of time
 - periods is based on (A) the value of the second component during the time
 - 4 period and (B) the value of the second component during at least one time
 - period adjacent to the time period.
3. The method of signal processing according to claim 1, wherein
 - 2 the series of time periods comprises a series of consecutive time periods of
 - equal duration.

4. The method of signal processing according to claim 3, wherein
2 a difference between the second time relation and the first time relation is
measured in durations of a time period and includes an integer portion and a
4 nonzero fractional portion, and

wherein the fractional portion is at least one-quarter of a time period
6 and no greater than three-quarters of a time period.

5. The method of signal processing according to claim 4, wherein
2 the fractional portion is substantially equal to one-half of a time period.

6. The method of signal processing according to claim 1, wherein
2 a boundary between each of the series of time periods is defined by a
transition of a clock signal.

7. The method of signal processing according to claim 6, wherein
2 a duty cycle of the clock signal is substantially equal to fifty percent.

8. The method of signal processing according to claim 1, wherein
2 the values multiplexed onto the common signal path are n bits wide, and
wherein the common signal path is less than $2n$ bits wide.

9. The method of signal processing according to claim 1, wherein
2 the values multiplexed onto the common signal path are n bits wide, and
wherein the common signal path is n bits wide.

10. The method of signal processing according to claim 1, further
2 comprising producing a delayed first component based on the first component
and having an integer delay with respect to the first component,

4 wherein multiplexing the values of the delayed second component and
a component based on the first component onto a common signal path includes
6 multiplexing the values of the delayed second component and the values of the
delayed first component onto a common signal path.

11. A method of signal processing, said method comprising:

2 receiving a composite signal having a first component and a
second component, the first component including a series of values, each
4 value of the first component being constant over substantially an entire
corresponding one of a series of time periods, the second component including
6 a series of values, each value of the second component being constant over
substantially an entire corresponding one of the series of time periods;

8 producing a delayed second component based on the second
component and having a fractional delay with respect to the second
10 component, the delayed second component including a series of values, each
value of the delayed second component being constant over substantially an
12 entire corresponding one of the series of time periods; and

multiplexing the delayed second component and the values of a
14 component based on the first component onto a common signal path.

12. The method of signal processing according to claim 11,
2 wherein the value of the delayed second component during each of the series
of time periods is based on (A) the value of the second component during the
4 time period and the (B) value of the second component during at least one
time period adjacent to the time period.

13. The method of signal processing according to claim 11,
2 wherein the series of time periods comprises a series of consecutive time periods of equal duration.

14. The method of signal processing according to claim 13,
2 wherein the fractional delay is measured in durations of a time period and includes an integer portion and a nonzero fractional portion, and
4 wherein the fractional portion is at least one-quarter of a time period and no greater than three-quarters of a time period.

15. The method of signal processing according to claim 14,
2 wherein the fractional portion is substantially equal to one-half of a time period.

16. The method of signal processing according to claim 11,
2 wherein a boundary between each of the series of time periods is defined by a transition of a clock signal.

17. The method of signal processing according to claim 16,
2 wherein a duty cycle of the clock signal is substantially equal to fifty percent.

2 18. The method of signal processing according to claim 11,
wherein the values multiplexed onto the common signal path are n bits wide,
4 and wherein the common signal path is less than $2n$ bits wide.

 19. The method of signal processing according to claim 11,
2 wherein the values multiplexed onto the common signal path are n bits wide,
and wherein the common signal path is n bits wide.

 20. The method of signal processing according to claim 11, further
2 comprising producing a delayed first component based on the first component
and having an integer delay with respect to the first component,
4 wherein multiplexing the values of the delayed second
component and the values of a component based on the first component onto a
6 common signal path includes multiplexing the values of the delayed second
component and the values of the delayed first component onto a common
8 signal path.

 21. The method of signal processing according to claim 11, further
2 comprising:

 demultiplexing the values of the delayed second component
4 and the values of the component based on the first component from the
common signal path to produce a transferred first component based on the first
6 component and a transferred second component based on the second
component; and

8 modulating an in-phase component of a carrier with a
component based on the transferred first component and a quadrature

10 component of the carrier with a component based on the transferred second
component.

22. The method of signal processing according to claim 11, further
2 comprising:

demultiplexing the values of the delayed second component
4 and the values of the component based on the first component from the
common signal path to produce a transferred first component based on the first
6 component and a transferred second component based on the second
component; and

8 producing a first analog component based on the transferred
first component and a second analog component based on the transferred
10 second component.

23. A method comprising:

2 receiving a first composite signal having a first component and
a second component; and

4 transmitting a second composite signal having a first
component and a second component,

6 wherein a stream of digital information carried over the first
component of the first composite signal is synchronous with a clock signal and
8 has a first time relation to a stream of digital information carried over the
second component of the first composite signal, and

10 wherein a stream of digital information carried over the first
component of the first composite signal is synchronous with the clock signal
12 and has a second time relation to a stream of digital information carried over
the second component of the second composite signal, and

14 wherein the stream of digital information carried over the first
component of the second composite signal is based on the stream of digital
16 information carried over the first component of the first composite signal, and

 wherein the stream of digital information carried over the
18 second component of the second composite signal is based on the stream of
digital information carried over the second component of the first composite
20 signal, and

 wherein the first time relation is different from the second time
22 relation.

24. The method of signal processing according to claim 23,
2 wherein the value of the second component of the second composite signal
during each period of the clock signal is based on (A) the value of the second
4 component of the second composite signal during the period of the clock
signal and (B) the value of the second component of the second composite
6 signal during at least one period of the clock signal adjacent to the period of
the clock signal.

25. The method of signal processing according to claim 23,
2 wherein a difference between the second time relation and the first time
relation is measured in durations of a period of the clock signal and includes
4 an integer portion and a nonzero fractional portion, and

 wherein the fractional portion is at least one-quarter of a period
6 of the clock signal and no greater than three-quarters of a period of the clock
signal.

26. The method of signal processing according to claim 25,
2 wherein the fractional portion is substantially equal to one-half of a period of the clock signal.

27. The method of signal processing according to claim 23,
2 wherein a duty cycle of the clock signal is substantially equal to fifty percent.

28. The method of signal processing according to claim 23,
2 wherein the values multiplexed onto the common signal path are n bits wide, and wherein the common signal path is less than $2n$ bits wide.

29. The method of signal processing according to claim 23,
2 wherein the values multiplexed onto the common signal path are n bits wide, and wherein the common signal path is n bits wide.

30. A device configured and arranged to output a multiplexed
2 signal based on an original composite signal having a first component and a second component, said device comprising:
4 a common signal path configured and arranged to carry the multiplexed signal;
6 a multiplexer configured and arranged to receive (A) a component based on the first component and (B) a delayed second component
8 based on the second component and to produce the multiplexed signal; and
a filter configured and arranged to receive the second
10 component and to produce the delayed second component.

2 31. The device according to claim 30, wherein the common signal
path includes a plurality of terminals of a chip package that includes the
4 device.

 32. The device according to claim 30, further comprising a delay
2 configured and arranged to receive the first component and to output a delayed
first component based on the first component,
4 wherein the multiplexer is configured and arranged to receive
the delayed first component.

 33. The device according to claim 30, wherein the first component
2 and the second component are synchronous to a clock signal, and wherein a
length of a delay of the delayed second component with respect to the second
4 component is measured in durations of a period of the clock signal and
includes an integer portion and a nonzero fractional portion, and

6 wherein the fractional portion is at least one-quarter of a period
of the clock signal and no greater than three-quarters of a period of the clock
8 signal.

 34. The device according to claim 30, wherein the fractional
2 portion is substantially equal to one-half of a period of the clock signal.

 35. The device according to claim 30, wherein the filter includes a
2 shifter configured and arranged to receive an input value and to output a

shifted value, wherein the shifted value is equal to 2^i times the input value,
 4 where i is an integer, and
 wherein a value of the delayed second component is based on
 6 the shifted value.

36. The device according to claim 30, wherein a transfer function
 2 of the filter is expressible as

$$(-1/16)z + (9/16)z^{-1} + (9/16)z^{-2} + (-1/16)z^{-3}.$$

37. A system including:

2 a device configured and arranged to output a multiplexed signal based
 on an original composite signal having a first component and a second
 4 component, said device comprising:

a common signal path configured and arranged to carry the
 6 multiplexed signal,

a multiplexer configured and arranged to receive (A) a
 8 component based on the first component and (B) a delayed second component
 based on the second component and to produce the multiplexed signal, and

10 a filter configured and arranged to receive the second
 component and to produce the delayed second component;

12 a demultiplexer configured and arranged to receive the
 multiplexed signal and to produce a transferred first component based on the
 14 first component and a transferred second component based on the delayed
 second component,

16 wherein the delayed second component is synchronous to the
first component and has a fractional delay with respect to the second
18 component.

38. The system according to claim 37, further comprising a
2 modulator configured and arranged to modulate an in-phase component of a
carrier with a component based on the transferred first component and a
4 quadrature component of the carrier with a component based on the
transferred second component.

39. The system according to claim 37, further comprising a first
2 digital-to-analog converter configured and arranged to produce a first analog
component based on the transferred first component and a second digital-to-
4 analog converter configured and arranged to produce a second analog
component based on the transferred second component.